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(71) Applicant: **INTERNATIONAL BUSINESS MACHINES CORPORATION**

**Armonk, NY 10504(US)**

(72) Inventor: **Grube, Gary W.**
**9 Oakwood Trail North**
**Washingtonville, N.Y. 10950(US)**
Inventor: **Khandros, Igor Y.**
**503 Furnace Dock Road**
**Peekskill, N.Y. 10566(US)**

(74) Representative: **Klocke, Peter, Dipl.-Ing. et al**
**IBM Deutschland GmbH Patentwesen und Urheberrecht Schönaicher Strasse 220**
**W-7030 Böblingen(DE)**

## (54) Direct attachment of semiconductor chips to a substrate with a thermoplastic interposer.

(57) A method for the direct attachment of semiconductor chips (10) to a substrate or module (12) with a polymer interposer (16). Initially, an interposer sheet (16) is fabricated, which is to be positioned between the chips (10) and the substrate (12), with via patterns conforming to the contact patterns of the chips (10). The interposer sheet (16) comprises a sheet of dielectric thermoplastic material selected from an elastomer, a filled elastomer, a polymer, or a copolymer. The chips (10) are then placed on the interposer sheet (16) with each chip (10) being positioned on a conforming via pattern, and the chips (10) are attached to the interposer sheet (16), as with a suitable adhesive. The vias are then filled with a conductive attachment material (24) comprising a solution of a thermoplastic polymer, preferably a copolymer of polyimide and siloxane, and a fine metal, preferably gold, forming a past . Th interposer sheet (16) with the attached chips (10) is then diced into individual chips (10), with ach chip (10) having a section of the interposer sh t (16) attached thereto. The chips (10) with attached interposer (16) are then directly attached to a substrate or module (12), with the interposer (16) therebetween, by applying heat and pressure, and the substrate (12) provides a controlled joint height and encapsulated joints.

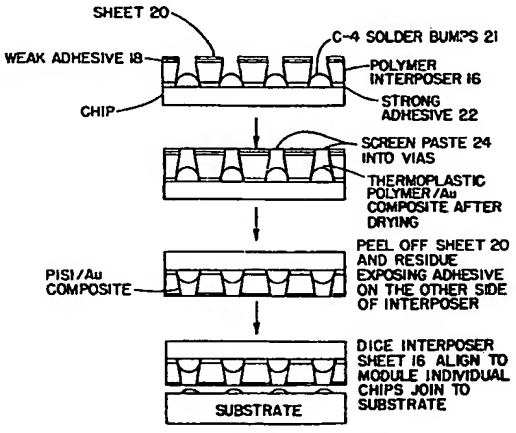


FIG.2

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The present invention relates generally to th direct attachment of semiconductor chips to a substrate or modul with th us of a th rmoplastic interposer therebetween. More particularly, the subject invention pertains to the direct attachment of s miconductor chips to a substrate or module with a thermoplastic polymer interposer and a joining material preferably formed of a composite of a thermoplastic polymer such as a copolymer of polyimide and siloxane and a fine metal such as gold powder.

Direct chip attachment of semiconductor chips to multichip modules has been practiced commercially, and offers obvious advantages in terms of d nsity and performance. Although there are advantages to direct chip attachment on multilayer c ramic (MLC) modules, there are also disadvantages associated therewith. High temperature solder is normally used for reliability related reasons for the electrical connections, with the joining temperature cycling up to 370°C, which limits the choice of materials which can be used in the components, particularly with respect to polymers.

Burn-in and testing of multichip modules is performed on a module populated with many chips. This results in a great deal of rework, and subsequent solder reflows over the entire module substrate, generally for the purpose of reattaching only one or two chips. Therefore, the multichip module, including metallurgies on both chip and substrate sid s thereof, is required to be designed to withstand ten to twenty reflow cycles. Accordingly, although this technology offers a number of advantages, it also has a number of disadvantages associated therewith.

The present invention incorporates some of the advantages of this existing technology which can use a controlled collapse chip connection (C-4) pattern on the chips, while alleviating several of the problems associated therewith.

Several U.S. Patents have been evaluated as prior art relative to the present invention, but all are quite distinct for the following reasons. U.S. Patent 4,648,179 fabricates an interconnection layer which is bonded to a module, but does not disclose or t ach chip interconnection/encapsulation. U.S. Patent 4,179,802 uses metal studs that have been lectroplated, and uses small amounts of solder to make the electrical connections which are essentially direct stud connections. In contrast thereto, the present invention preferably uses a metal-polym r composite to provide the electrical connections, and provides encapsulat d connections joining th chip to th substrat . U.S. Pat nt 4,642,889 uses fine wires which are positioned within a paper interposer surrounded by solder and flux, which are then h at d and melted to mak th el ctrical connections. Afterwards, the paper interposer is totally removed by dissolving it in a washing operation. In contrast thereto, the pres nt invention uses th int rposer to both join and ncapsulat the chip to a substrate or module.

Accordingly, it is a primary object of the present invention to provide for the direct attachment of semiconductor chips to a substrate or module with the use of a thermoplastic interposer therebetween.

The present invention as claimed provides a fluxless, low temperature, direct chip attachment method and structure based upon the use of a diceable thermoplastic interposer permanently attached to a chip which:

provides well controlled and easily adjusted contact joint heights;

produces encapsulated contact joints with increased resistance against thermal fatigue failure;

facilitates temporary contact for chip burn-in with a flat interposer and with substantially no C-4 pattern height variation;

can be used with a variety of joining metallurgies, including a poly[imide-siloxane]/gold composite which does not require the use of a flux, or with solder or other suitable materials;

reduces traditional requirements imposed on contact metallurgies for C-4 patterns, thus reducing bonding, assembly and testing costs for direct chip attachment;

and

is inexpensive and easily manufacturable.

In accordance with the teachings herein, the present invention provides a method of direct attachment of semiconductor chips to a substrate or module. In a preferred embodiment disclosed herein, a plurality of chips are prepared for subsequent attachment to a substrate or module by starting with a large interposer sheet to which a plurality of chips are attached and which is subsequently diced to form individual chips, each having a section of the interposer sheet attached thereto. However, the present invention is also applicable to the preparation of a single chip with a corresponding interposer prepared as described herein. In the disclosed embodiment wherein a plurality of chips are prepared on an interposer sheet, initially, the interposer sheet is fabricated, which is to be positioned between the chips and the substrate, with via patterns therein conforming to the contact patterns of the chips. The chips are then placed on the interposer sheet with each chip being positioned over a conforming via pattern, and the chips are attached to th interposer sheet, as with a suitable adh sive. Th vias ar th n filled with a conductiv attachment mat rial. Th int rposer she t with the attached chips is then diced into individual chips, with ach chip having a section of th int rposer sheet attached thereto. The chips with attached

interposer are then directly attached to a substrat or module, with th interposer therebetween, by applying h at and pr ssure, and th interpos r provides a controlled contact joint height and encapsulated contact joints.

In greater detail, in preferred embodiments the vias are filled with a conductive attachment composite material comprising a thermoplastic solution of a thermoplastic polymer, preferably a copolymer of polyimide and siloxane, and a fine metal, preferably gold, forming a paste. The interposer sheet comprises a sheet of thermoplastic dielectric material selected from an elastomer, a filled lastomer, a thermoplastic polymer, or a thermoplastic copolymer, and the interposer sheet and conductive attachment material are preferably sel cted to have matching properties, particularly with respect to their coefficients of thermal expansion. In the fabrication of the interposer sheet, the sheet can be preferably laser ablated, or alternatively punched or drilled, to create via patterns matching the contact patterns of the chips. The chips are attached to the interposer sheet with a first adhesive, and the chips are attached to the substrate or module with a second adhesive which is not as strong in bonding strength as the first adhesive. This feature provides for rework in which the second adhesive is ruptured to detach the chip from the substrate or module while the first adhesive r mains intact.

Following the step of filling the vias with a conductive attachment material, the chips may be burned-in and tested by contacting a burn-in module. The burn-in module is provided with a bump for each via, and the radius of each bump on the burn-in module is preferably larger than the radius of bumps of conductive attachment material provided on the substrate to ensure adequate composite flow during the step of direct attachment of the chips to the substrate or module.

The foregoing objects and advantages of the present invention for direct attachment of semiconductor chips to a substrate with a thermoplastic interposer may be more readily understood by one skilled in the art with reference being had to the following detailed description of several preferred embodiments thereof, taken in conjunction with the accompanying drawings wherein like elements are designated by identical reference numerals throughout the several views, and in which:

Fig. 1 illustrates a method for joining a semiconductor chip to a substrate utilizing a poly[imide- siloxane]/gold composite joining mat rial which does not us sold r and is fluxless, and in which joining is performed above Tg (the glass transition temperature) of th composit copolymer;

Fig. 2 shows the sequenc of st ps involv d in th use of an interpos r pursuant to th t achings of the pr sent inv ntion, which provides controlled joint height and joint encapsulation, and in which a poly[imide-siloxane]/gold composite paste is used as the electrical/mechanical attachment material;

Fig. 3 shows the direct attachment of a composite bumped chip to a substrate with an interposer therebetween and a poly[imide-siloxane]/gold composite joining material, and also shows the hierarchy of adhesives provided for rework;

Fig. 4 illustrates the direct attachment of a chip without solder or composite bumps to a substrate with an interposer therebetween and a poly[imide-siloxane]/gold composite joining material which provides solderless, fluxless, encapsulated joints;

Fig. 5 depicts a burn-in of a chip on a thermoplastic interposer by temporary mechanical contact with a burn-in module;

Fig. 6 shows the attachment of a burned-in chip, diced from the interposer sheet, to a multichip module; and

Fig. 7 illustrates a method of locally reapplying a composite joining material paste pattern to a substrate for attachment of a replacement chip during rework.

Fig. 1 illustrates a method for joining a semiconductor chip 10 to a substrate or module 12 utilizing a poly[imide-siloxane]/gold composite joining material which is applied as patterns of C-4 bumps 14 on both the chip and the substrate. Advantageously, this method does not use solder and is fluxless, and joining is performed above Tg (the glass transition temperature) of the composite copolymer. In such a direct chip attachment method, pressure is applied between the chip and module during the joining process. With this approach, it is difficult to precisely control the height of each contact bump forming each electrical contact joint, which in turn can result in an increase in effective thermal fatigue stresses.

The present invention allows the electrical contact joint heights to be precisely controlled by introducing an int rposer 16 betwe n th semiconductor chip and th substrat or modul . Fig. 2 shows the sequence of steps involv d in using an interposer pursuant to the teachings of th present inv ntion, which provid s controll d joint h ight and joint encapsulation, and in which a poly[imide-

siloxane]/gold composite paste is used as th electrical/m chanical attachment mat rial.

Th int rpos r 16 can b fabricat d from a sheet, typically 203 to 254 microns (8 to 10 mils) thick, of a thermoplastic dielectric material. The interposer 16 is thermoplastic to facilitate the initial attachment process and also to provide for rework and detachment of a chip from the substrate or module, and is dielectric to electrically insulate the electrical contact joints. The interposer sheet can be fabricated from a thermoplastic dielectric lastomer such as silicone, a filled elastomer for dimensional control (with typical fillers being di lectrics such as glass, ceramic, aluminum nitride or any other suitable dielectric filler material), a thermoplastic dielectric polymer or copolymer such as polyimide and siloxane, or other various polymers and copolymers. A copolymer of polyimide and siloxane, as is available commercially from G neral Electric, is preferred wherein siloxane is present in 10 to 20% of the molecular chain, and provides an adhesive quality for the copolymer.

Initially, a large area interposer sheet is fabricated with a layer of a relatively weak adhesive 18 covered by a peel off sheet 20 on one side and a lay r of a stronger adhesive 22 on the opposite sid . The interposer sheet is then preferably laser ablated, or alternatively punched or drilled, for personalization to create via patterns conforming to the C-4 patterns of chips to be joined, with each via typically having a diameter between 200 and 250 microns. Chips with solder bumps 21, as in Fig. 2, or with composite bumps 23 as in Fig. 3, are then placed on top of the strong adhesive layer 22 on th interposer sheet with the solder or composite bumps being positioned in the vias without a requirement for precise alignment, and permanently adhere to the adhesive on top of the interposer sheet with a strong adhesion.

The direct chip attachment is preferably accomplished with a thermoplastic polymer such as the copolymer poly[imide- siloxane] mixed with a conductive fine metal to form a composite paste 24. The paste 24 can consist of a solution of a th rmoplastic polymer, preferably, but not limited to, a copolymer of polyimide and siloxane mixed with fine metal, preferably gold, or gold coated metal, polymer or ceramic, to form a screenable paste. The metal provides conductivity for the electric contact joints and can be any suitable fine m tal such as gold or silver. Gold is preferred, such as product 1800 powder available from Metz M tallurgical Corp., South Plainfield, N.J. 07080, which is a copr cipitat d sph r and flak mixtur having a 2.2u averag particle size. Th gold powder is pr ferably mixed with a polyimide and siloxan copolym r having from 30% to 70%, pref rably 50%, gold powder by volume. Poly[imide-siloxane] copolymers that hav been us d for joining hav Tg's varying between 100 and 250°C, with joining t mp ratur s ranging from 200 to 380°C.

The interposer sheet populated with chips prepared as indicated hereinabove is then turned over to the position illustrated in the top of Fig. 2, and the composite paste 24 is screened into the vias and the excess paste wiped off as shown in the second stage of Fig. 2. The paste residue is then removed by peeling off the sheet 20, thereby exposing the weak adhesive 18 as shown in the third stage of Fig. 2. The interposer sheet with chips thereon can then be diced, and the chips with interposers at the bottom are then individually attached, as illustrated in the fourth stage of Fig. 2 and also in Fig.s 3 and 4.

Fig. 3 shows the direct attachment of a composite bumped 23 chip with an interposer and a poly[imide-siloxane]/gold composite, and also shows the hierarchy of adhesives provided for rework. Fig. 4 illustrates the direct attachment of a chip without solder or composite bumps to a substrate with an interposer and a poly[imide-siloxane]/gold composite which provides solderless, fluxless, encapsulated joints. An advantage of the embodiment of Fig. 4 is that the step of applying solder or composite contact bumps to the chips is eliminated.

Either subsequent to dicing or prior to dicing, the interposer sheet can be used to burn-in and electrically test the chips by contacting a burn-in module 25, which could be a multilayer ceramic (MLC) burn-in module. The simultaneous contact of pads on a module is possible because of the designed flat bottom of the interposer sheet. The C-4 pattern ball height variations, which might occur in the structure of Fig. 1, has thus been eliminated.

Fig. 5 depicts a burn-in of chips on an interposer by temporary mechanical contact with an MLC burn-in module 25. Following the burn-in, and as described hereinabove, the interposer sheet with chips is diced, and the individual chips are ready for direct chip attachment as shown in Fig.s 2, 3 and 4. To ensure reliable bonding with metallurgy filled vias, preferably with a poly[imide-siloxane]-/gold composite, the radius of bumps 26 on the burn-in module 25 should be larger than the radius of paste bumps 28 on the substrate, as shown in Fig. 6, which illustrates the attachment of burned-in chips diced from the interposer to a multichip module. The larg r radius ensures an adequate amount of composit flow during th dir ct chip attachment.

Th int rposer structure is also compatibl with and in alt rnativ mbodim nts can b used with a metal solder via fill instead of a conductiv com-

posite via fill, but is limited to fluxes which do not chemically react with and alter the material of the interposer. The metal solder can be applied using a solder wave and related techniques. The use of a low temperature solder in the vias ensures low temperature attachment to a substrate.

The properties of the interposer material are preferably selected to match those of the poly-[imide-siloxane]/gold composite or other joining material used in conjunction with the interposer, particularly with respect to their coefficients of thermal expansion, such that the interposer also functions as an effective encapsulant. Preferably, both are formed of the same polymer such as the copolymer polyimide and siloxane. With such matching properties, the interposer distributes the stresses along the entire chip/substrate area, effectively lowering stresses on the joints, which has proven to significantly increase resistance to thermal fatigue.

Considering and providing for rework, two adhesives 18 and 22 are employed in the joining process, as shown in Fig.s 2, 3 and 4. The adhesive 22 between the chip and the interposer is selected to have a higher bonding strength than the adhesive 18 between the interposer and the substrate. As a result, when a chip is being removed for rework, the interposer/substrate interface is always the one to fracture. Any remaining adhesive can be removed by locally wiping the residual paste and polymer with a solvent. In embodiments wherein no adhesive is used between the interposer and the substrate, and the substrate/interposer joining is by the thermoplastic and adhesive properties of the interposer material, the soluble polymer is removed in the same fashion.

To join a replacement chip, a pattern of poly-[imide-siloxane]/gold paste can be applied locally to a substrate or module. This is difficult to do by screening. However, the pattern can be applied by a silicon pad, which picks up the wet pattern through a screen, and deposits it locally onto C-4 pattern pads, as depicted in Fig. 7, which illustrates a method of locally reapplying a paste pattern to a substrate.

While several embodiments and variations of the present invention for direct attachment of semiconductor chips to a substrate with a thermoplastic interposer are described in detail herein, it should be apparent that the disclosure and teachings of the present invention will suggest many alternative designs to those skilled in the art.

## Claims

1. A method of direct attachment of semiconductor chips (10) to a substrate or module (12), comprising:
   a) fabricating a thermoplastic and dielectric interposer (16), which is to be positioned between the chip (10) and the substrate (12), with a via pattern matching the contact pattern of the chip (10);
   b) placing the chip (10) on the interposer (16) with the contact pattern of the chip (10) being positioned on the matching via pattern, and attaching the chip (10) to the interposer (16);
   c) filling the vias of the interposer (16) with a conductive attachment material; and
   d) directly attaching the chip (10) with attached interposer (16) to a substrate or module (12), with the interposer (16) therebetween, with the interposer (16) providing a controlled joint height and providing encapsulated joints.

2. A method of direct attachment of semiconductor chips (10) to a substrate or module (12) as claimed in claim 1, wherein:
   a) said step of fabricating comprises fabricating a thermoplastic and dielectric interposer sheet (16), which is to be positioned between a plurality of chips (10) and the substrate (12), with via patterns matching the contact patterns of the chips (10);
   b) said step of placing comprises placing the chips (10) on the interposer sheet (16) with each chip (10) being positioned on a matching via pattern, and attaching the chip (10) to the interposer sheet;
   c) said step of filling comprises filling the vias on the interposer sheet (16) with a conductive attachment material (24); and
   d) dicing the interposer sheet (16) with the attached chips (10) into individual chips (10), with each chip having a section of the interposer sheet (16) attached thereto.

3. A method of direct attachment of semiconductor chips (10) to a substrate or module (12) as claimed in claim 1 or claim 2, wherein the vias are filled with a conductive attachment material (24) comprising a solution of a thermoplastic polymer, preferably a copolymer of polyimide and siloxane, and a conductive fine metal, preferably gold, forming a paste.

4. A method of direct attachment of semiconductor chips (10) to a substrate or module (12) as claimed in anyone of the preceding claims, wherein the interposer (16) is formed of a material selected from an elastomer, a filled elastomer, a thermoplastic polymer, and a thermoplastic copolymer.

5. A method of direct attachment of semiconductor chips (10) to a substrate or module (12) as claimed in claim 4, wh r in th interposer (16) and conductive attachment materials are similar materials having matching properties and matching coefficients of thermal expansion.

6. A method of direct attachment of semiconductor chips (10) to a substrate or module (12) as claimed in anyone of the preceding claims, wherein said step of fabricating the interposer (16) includes fabricating the interposer (16) with a layer of relatively weak adhesive (18) on one side for attaching the interposer (16) to a substrate or module (12), covered by a peel off sheet (20), and with a layer of relatively strong adhesive (22) on a second side for attaching chips (10) to the interposer (16).

7. A method of direct attachment of semiconductor chips (10) to a substrate or module (12) as claimed in claim 6, wherein said step of fabricating the interposer (16) includes laser ablating the interposer (16) to create via patterns matching the contact patterns of the chips.

8. A method of direct attachment of semiconductor chips (10) to a substrate or module (12) as claimed in anyone of the preceding claims, wherein the chip (10) is attached to the interposer (16) with a first adhesive (22).

9. A method of direct attachment of semiconductor chips (10) to a substrate or module (12) as claimed in claim 8, wherein the chip (10) is attached to the substrate or module (12) with a second adhesive (18) which is not as strong in bonding strength as the first adhesive (22), to provide for rework in which the second adhesive (18) is ruptured to detach the chip (10) from the substrate or module (12) while the first adhesive (22) remains intact.

10. A method of direct attachment of semiconductor chips (10) to a substrate or module (12) as claimed in claim 9, wherein following rupture, a pattern of conductive attachment material (24) is applied locally onto the substrate or module (12).

11. A method of direct attachment of semiconductor chips (10) to a substrate or module (12) as claim d in anyon of th preceding claims, wher in following th filling step, th chip (10) is burned-in by contacting a burn-in module (25).

12. A method of direct attachm nt of s miconductor chips (10) to a substrate or module (12) as claim d in claim 11, wher in th burn-in module (25) is provided with a bump (26) for each via, and the radius of each bump (26) on the burn-in module (25) is larger than the radius of bumps (28) of conductive attachment material (24) provided on the substrate or module (12) to ensure adequate composite flow during the step of directly attaching.

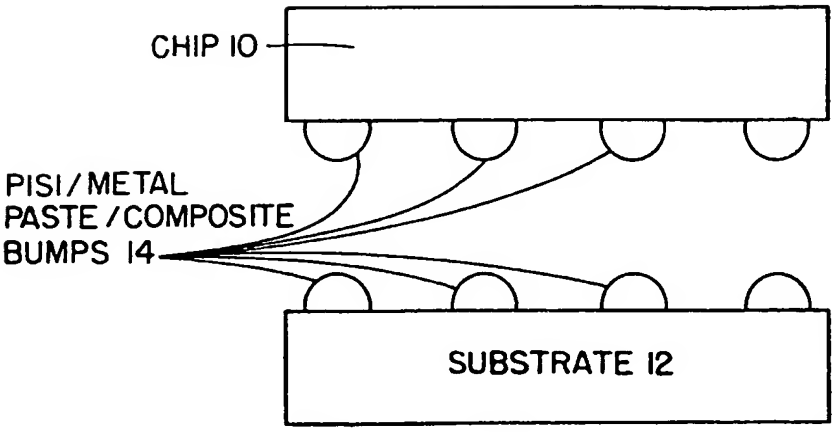

CHIP 10
PISI/METAL PASTE/COMPOSITE BUMPS 14
SUBSTRATE 12

FIG.1

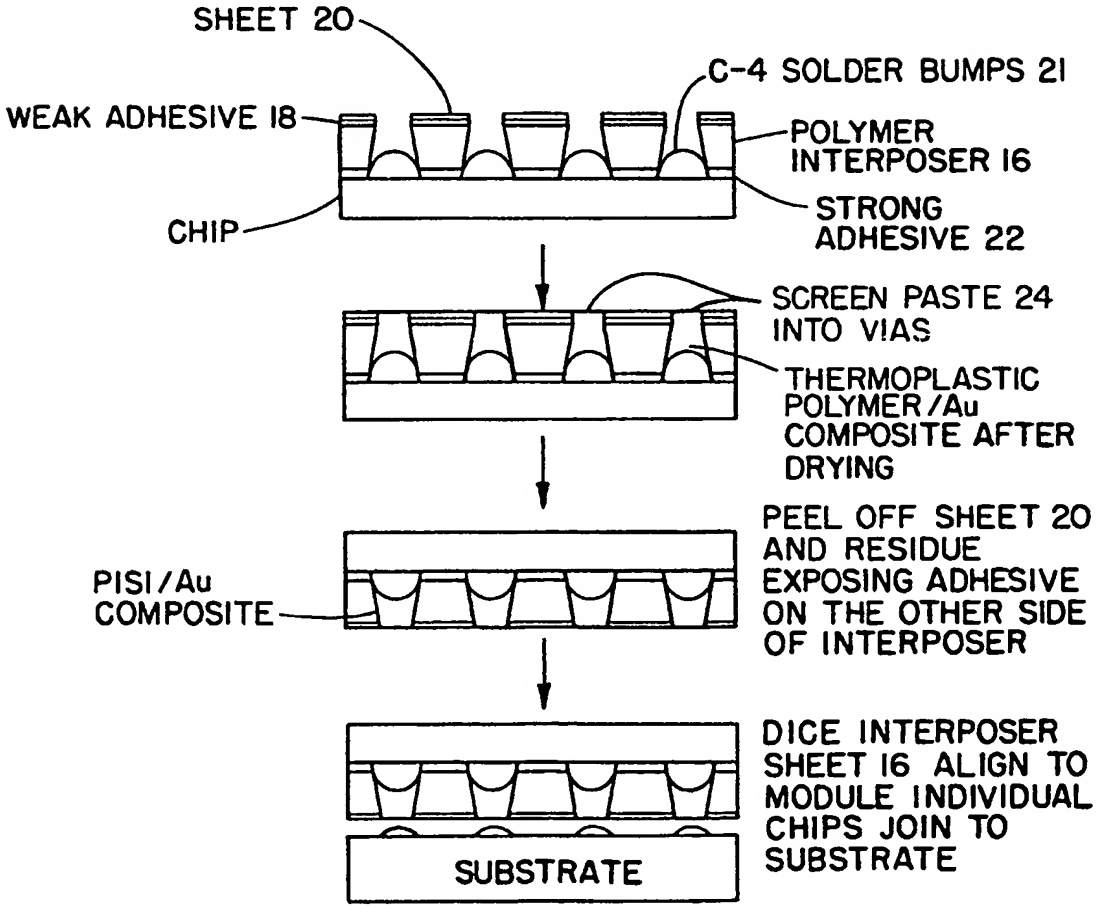

SHEET 20
C-4 SOLDER BUMPS 21
WEAK ADHESIVE 18
POLYMER INTERPOSER 16
CHIP
STRONG ADHESIVE 22
SCREEN PASTE 24 INTO VIAS
THERMOPLASTIC POLYMER/Au COMPOSITE AFTER DRYING
PEEL OFF SHEET 20 AND RESIDUE EXPOSING ADHESIVE ON THE OTHER SIDE OF INTERPOSER
PISI/Au COMPOSITE
DICE INTERPOSER SHEET 16 ALIGN TO MODULE INDIVIDUAL CHIPS JOIN TO SUBSTRATE
SUBSTRATE

FIG.2

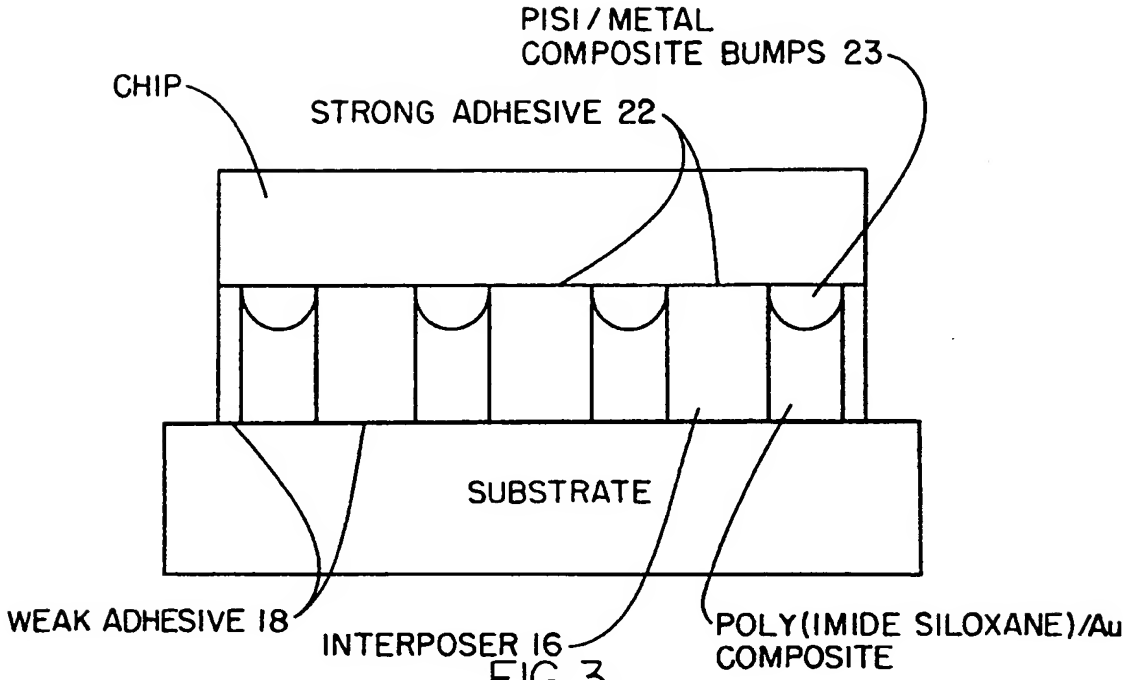

PISI / METAL
COMPOSITE BUMPS 23
CHIP
STRONG ADHESIVE 22
SUBSTRATE
WEAK ADHESIVE 18
INTERPOSER 16
POLY(IMIDE SILOXANE)/Au
COMPOSITE

FIG.3

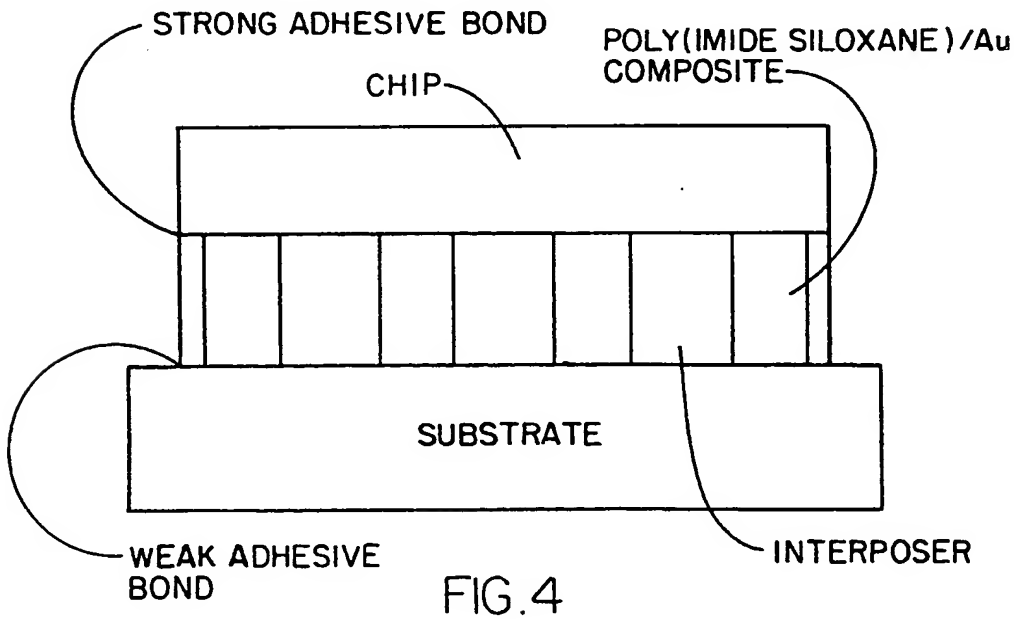

STRONG ADHESIVE BOND
POLY(IMIDE SILOXANE)/Au
COMPOSITE
CHIP
SUBSTRATE
WEAK ADHESIVE
BOND
INTERPOSER

FIG.4

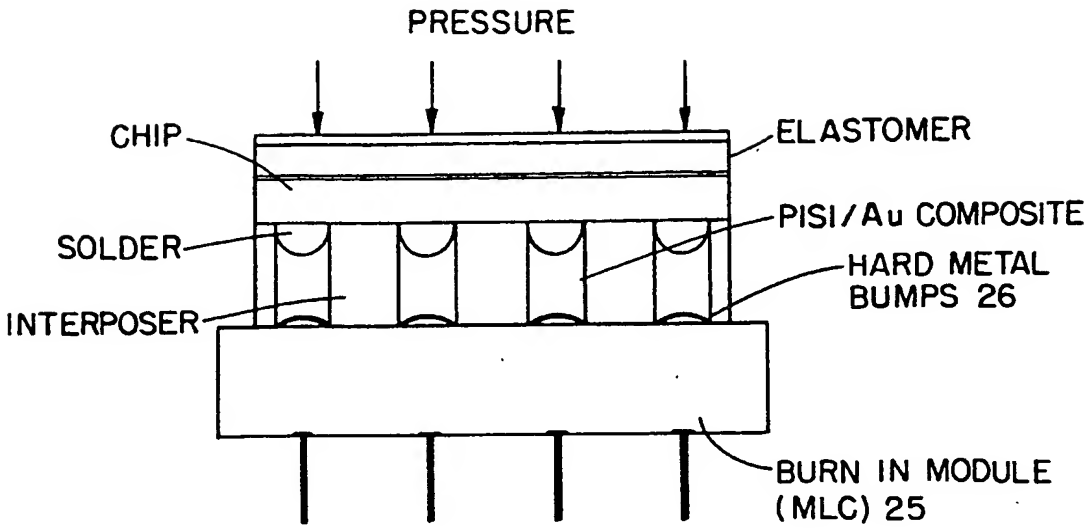

PRESSURE
CHIP
ELASTOMER
PISI/Au COMPOSITE
SOLDER
HARD METAL
BUMPS 26
INTERPOSER
BURN IN MODULE
(MLC) 25

FIG.5

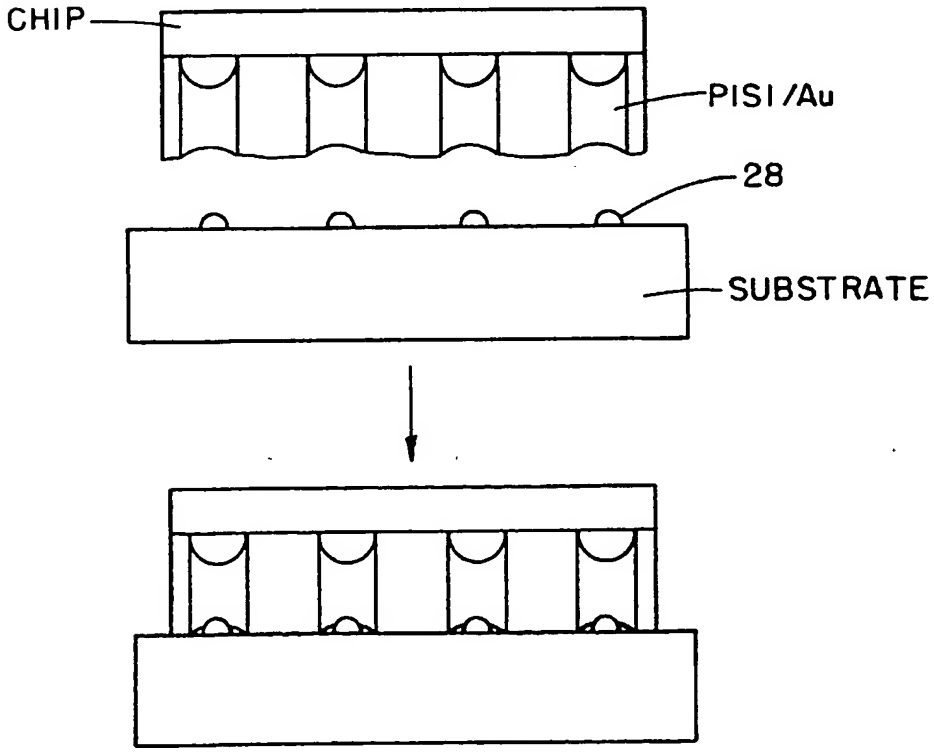
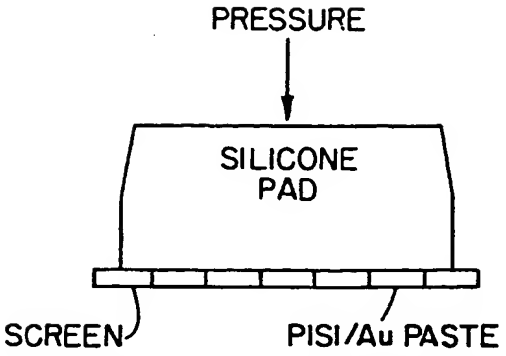
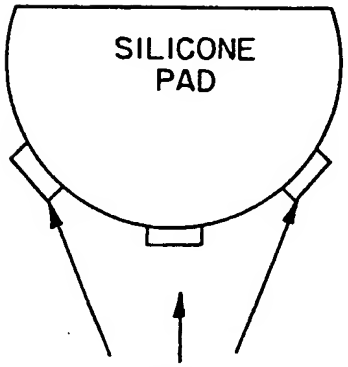

CHIP
PISI/Au
28
SUBSTRATE

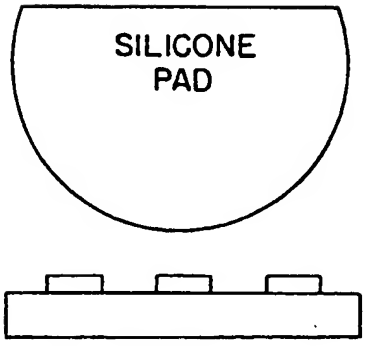
FIG.6




1. PASTE BUMPS PICKED-UP BY SILICONE PAD




2. BUMPS REMAIN ON PAD




3. BUMPS ARE TRANSFERED ONTO A SUBSTRATE

FIG. 7

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 91 11 2075

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| X | PATENT ABSTRACTS OF JAPAN<br>vol. 9, no. 110 (E-314)(1833) 15 May 1985<br>& JP-A-60 001 849 ( SHARP K.K. ) | 1-3,5 | H01L23/498 |
| Y | * abstract * | 4 | |
| Y | EP-A-0 284 820 (CANON KABUSHIKI KAISHA) | 4 | |
| A | * column 2, line 28 - line 51; figures 5,6 *<br>* column 16, line 5 - line 29 *<br>* column 16, line 56 - column 17, line 40; claims *<br>*embodiment 155* | 6-8 | |
| A | EP-A-0 344 719 (CANON KABUSHIKI KAISHA)<br>*col.12, "(Removeable connection)"* | 6,8-10 | |
| A | 36th ECC,May5-7,1986,IEEE 0569-5503/86/0000-0285<br>pp.285-295,L. YING:"A Novel Approach ----<br>Thermoplastic Die Attach Adhesive" | | |
| P,X | WO-A-9 109 419 (EPOXY TECHNOLOGY INC.)<br>* the whole document * | 1-5 | TECHNICAL FIELDS SEARCHED (Int. Cl.5)<br>H01L |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 21 NOVEMBER 1991 | PROHASKA G.A. |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)